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[METHOD AND STRUCTURE TO SUPPRESS EXTERNAL LATCH-UP]

Abstract

A method and structure for protection against latch-up is provided. Integrated circuits manufactured in accordance with the present disclosure feature well and substrate contacts of varying periodicity. Such a strategy enables maximizing the design of an integrated circuit as to the suppression of latch-up while concurrently optimizing available area on the chip allocable to circuit design. This method and structure is particularly beneficial to protect against cable discharge events and other discharge occurrences prone to injecting large current densities into an integrated circuit.